In the claims:

Please delete existing claims 1-39.

Please add the following set of claims:

1. A method for sampling at least one analog input signal, comprising:

(a) feeding a system with said at least one analog input signal and a plurality of discrete correction signals;

(b) said system providing analog monitoring outputs,

wherein said at least one analog input signal and said discrete correction signals are jointly related by a relationship to said analog monitoring outputs by a model having an identification algorithm;

(c) receiving said analog monitoring outputs and a synchronization clock and implementing a negative feedback control loop by said feeding said system with said discrete correction signals, in order to keep at least one of said analog monitoring outputs to be within a previously defined constraint;

(d) identifying said model, by creating an internal representation of said relationship;

(e) calculating a digital output signal by using a digital representation of said discrete correction signals and said model, wherein said digital output signal represents said at least one analog input signal.

2. The method of claim 1, wherein said system is selected from the group consisting of continuous systems, systems having a unified model, and continuous systems having a unified model.

3. The method of claim 1, wherein said system is time varying according to said synchronization clock.

4. The method of claim 1, wherein the value of said discrete correction signals is selected from the group consisting of at least two previously defined values, and at least two previously defined waveforms.

5. The method of claim 1, wherein said system is a linear system.

6. The method of claim 5, wherein said identifying includes a least- mean square (LMS) technique.7. The method of claim 1, wherein said calculating is only up to a previously defined partial reconstruction of said at least one analog input signal.

8. The method of claim 1, wherein said identifying is repeated occasionally within a training period, and said identifying includes feeding at least one analog training signal during said training period.

9 The method of claim 8, wherein said at least one analog signal is produced by feeding known digital signals to a digital to analog converter, said known digital signals driving said at least one analog training signal.

10. The method of claim 8, where said identifying is performed in the background by interleaving said at least one analog input signal and said at least one analog training signal.

11 The method of claim 1, wherein said identifying uses available statistical information about said at least one analog input signal.

12 The method of claim 8, wherein said at least one analog training signal is produced by at least one additional system fed by a known digital reference signal and said identifying includes a joint model identification algorithm.

13. A method for sampling at least one analog input signal by a multi-stage sampler including a plurality of stages, each stage including a system, the method comprising:

(a) providing for each said stage, except the first stage, the system receiving as input signals at least one analog signal from a preceding stage and at least one discrete correction signal;

(b) the system of the first stage receiving at least one discrete correction signal and at least one analog input signal;

(c) for each said stage, the system providing at least one analog monitoring output,

(d) providing, for each stage of said sampler, said at least one discrete correction signal, by using information from other stages said information including at least one analog monitoring output, and by further using a synchronization clock, wherein said at least one

discrete correction signal performs a negative feedback control loop in order to control said at least one analog monitoring output;

(e) receiving and storing from each said stage, a digital representation of said at least one discrete correction signal; and

(f) identifying a multi-stage sampler model of said multi-stage sampler, by identifying a plurality of unknown parameters within said multi-stage sampler model, thereby creating an internal representation of a relationship between a digital representation of the discrete correction signals of all stages of said multi-stage sampler, to the at least one analog input signal of said multi-stage sampler;

(g) reconstructing a digital output signal using said digital representation, and said multi-stage sampler model, wherein said digital output signal represents the at least one analog input signal of said multi-stage sampler.

14. The method of claim 13, wherein operation of each stage is dependent on at least one other stage.

15. A multi-stage analog signals sampler, wherein each stage of the multi-stage analog signals sampler includes:

(a) an amplifier which amplifies an input analog signal, thereby producing an amplified analog signal;

(b) a mechanism which at least approximately integrates said amplified analog signal, thereby producing an integrated signal;

(c) a mechanism which causes decaying of said integrated signal; and

(d) a mechanism which performs a comparison of said integrated signal with at least one threshold, and adds at least one previously defined correction to said amplified analog signal, and registers an output of said comparison in a digital logic.

16. A multi-stage analog signals sampler, wherein each stage of said multi-stage analog signals sampler includes:

(a) an amplifier amplifying an analog input signal, thereby producing an amplified analog signal;

(b) a mechanism which renders said amplifier dependent on a synchronization clock;

(c) a circuit which features a time constant on the order of a period of said synchronization clock, wherein said circuit modifies said amplified analog signal;

(d) a mechanism which provides, at least one discrete correction signal to said analog input signal, by using information from at least one other said stage, wherein said at least one discrete correction signal performs a negative feedback control loop which controls said analog input signal; and

(e) a mechanism which receives and stores, a digital representation of said at least one discrete correction signal.

17. The multi-stage analog signals sampler, according to claim 16, further comprising

(f) a mechanism which identifies a model of said multi-stage analog signals sampler,

(g) a digital signal processing mechanism which calculates a digital output signal representing said analog input signal.

18. A parallel analog signals sampler, comprising a plurality of the multi-stage analog signals samplers according to claim 16, wherein the respective digital representations of the multi-stage signal samplers are output to a common digital signal processing mechanism, the parallel analog signals sampler comprising a mechanism which identifies a joint model of said multi-stage analog signals samplers.

19. The parallel multi-stage analog signals sampler, according to claim 18, wherein said multi-stage analog signals samplers are placed in close proximity, wherein crosstalk between said parallel analog signal samplers is included in said joint model.

Respectfully Submitted,

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